Docket No.: P2002,0856

CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of German application DE 102 46 789.7, filed with the German Patent Office on October 8, 2002.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Description

Circuit arrangement and method for measuring at least one operating parameter for an integrated circuit

The present invention relates to a circuit arrangement and a method for measuring at least one operating parameter for an integrated circuit.

Integrated circuits can have different operating states which result, in particular, from their being operated in different operating states. By way of example, in an integrated memory circuit, it is possible to distinguish between a read operation and a write operation which have different circuit parts in operation, depending on the design of the memory. In addition, different operating states in a memory, for example, can result from write or read access involving access to different memory areas or to a different number of memory banks.

The operating states of an integrated circuit are generally specified in a datasheet. In this context, there is the problem that a precise operating state in which an electrical or physical parameter for the circuit needs to be determined is often not specified accurately enough. When stipulating operating states for specifying parameters in datasheets, it is often possible to establish differences particularly between the manufacturers of integrated circuits. In particular, it is often not possible to compare, by way of example, operating currents in integrated circuits from different manufacturers with one another directly if a manufacturer A takes into account a different side effect in

the measurement than a manufacturer B, who does not include such a side effect in the measurement. A similar situation applies when ascertaining operating temperatures or when ascertaining the power consumption of an integrated circuit.

So that it is possible to establish beyond doubt that an integrated circuit is operating correctly, the integrated circuit is generally subjected to a function test during the manufacturing process. Particularly in a test mode for an integrated memory, it is necessary to test the memory as close to the application as possible. In this case, the memory is usually tested under various operating conditions. To this end, by way of example, prescribed data values are written to memory cells in the memory cell array and are then read again in order that they can be compared with the prescribed data values. In this context, it has generally not been possible to date to compare a characteristic mode of operation for the application with the mode of operation of the function test directly in order to be able to establish whether the integrated circuit has been tested close to the application. In particular, it has not yet been possible to date to obtain a reliable statement as to whether the integrated circuit has gone through all the integrated circuit's operating modes in the function test during the manufacturing process in the same manner as in the subsequent application.

Diverse areas of use, particularly for integrated memory circuits in PDAs (Personal Digital Assistants), mobile telephones and other applications, and an ever faster growing product diversity mean that it would be of great benefit to be able to ascertain an operating parameter for an integrated circuit easily, particularly during operation of the circuit, in the application, in order to be able to trace application-specific operating conditions. Such operating parameters could

represent an aid to determining the test coverage of a function test.

The object of the present invention is to provide a circuit arrangement for measuring at least one operating parameter for an integrated circuit which can easily be used to ascertain an operating parameter for an integrated circuit during operation of the circuit in the application.

It is also an object of the present invention to specify a corresponding method for measuring at least one operating parameter for an integrated circuit.

This object is achieved by a circuit arrangement for measuring at least one operating parameter for an integrated circuit in accordance with patent claim 1 and by a method for measuring at least one operating parameter for an integrated circuit in accordance with patent claim 8.

The inventive circuit arrangement has an analysis circuit which is connected to at least one external connection on the integrated circuit. The analysis circuit detects a plurality of voltage level changes on an external connection on the integrated circuit and supplies them to a counter circuit. In this way, the counter circuit logs a digitally coded value which characterizes at least one operating parameter for the integrated circuit. An output circuit is connected to the analysis circuit and is used for externally outputting the coded value or a value derived therefrom, particularly an averaged value.

This means that voltage level changes on external connections on an integrated circuit, which are used to control a mode of operation for the integrated circuit, in particular, can be

logged in an instruction coded or pin coded form, for example, and can subsequently be digitally averaged in registers and output, in particular. This makes it advantageously possible to log an average mode of operation for the integrated circuit on the basis of a characteristic set of parameters and to ascertain respective operating states therefrom. The logged parameters can be output via the output circuit with a suitable log on request.

The analysis circuit can be provided externally (for example as a "flip chip"), internally, for example in a "package", or else in the form of an integrated circuit on the silicon. In this case, an internal circuit has the advantage that the signals can be tapped off from the signal paths largely without interference and that the analysis circuit has already been implemented on large scale integrated platforms as well. An external circuit has the advantage that the analysis circuit would need to be connected to the integrated circuit only when required.

To ascertain a characteristic set of parameters, the analysis circuit in one embodiment of the invention is connected to a plurality of external connections on the integrated circuit and also has a plurality of counter circuits. Each of the counter circuits is connected to one or more of the external connections via a different combinational logic circuit and respectively logs at least one digitally coded value. Hence, the analysis circuit detects a plurality of voltage level changes on the external connections in different ways, so that a plurality of different operating parameters can be ascertained from the digitally coded values.

In one advantageous development of the invention, the analysis circuit has a time counter circuit which is connected to a

connection for a clock signal and is used to log a defined period of time. The provision of such a time counter circuit makes it possible to log the average mode of operation of the integrated circuit. To this end, the digitally coded value(s) on the corresponding counter circuit are related to the averaging time logged using the time counter circuit. Averaging the digitally coded values allows more meaningful operating parameters for the integrated circuit to be obtained in defined cases.

In this regard, it is particularly advantageous if, upon reaching an averaging time which is a binary multiple during the measurement, the respective coded value logged up till then is related to this averaging time. This allows more precise averaging, since exact division by the averaging time which is a binary multiple is possible. The coded value logged up till then is advantageously copied to a respective register circuit, which is associated with a respective counter circuit, and is stored there and is available for the next division operation with the averaging time without the measurement needing to be stopped for this purpose. In addition, it advantageously allows the respective stored value to be used for logged output at all times.

Other advantageous embodiments and developments of the invention are specified in subclaims.

The invention is explained in more detail below with reference to the Fig. which is shown in the drawing.

The Fig. shows an advantageous embodiment of an inventive circuit arrangement for measuring an operating parameter for an integrated circuit. This example shows external connections P0 to P2 on an integrated circuit which are used to control a

method of operation for the integrated circuit. The connections P0 to P2 are in the form of instruction connections or address connections, for example. The number of external connections which can be evaluated is unlimited in principle. In addition, the integrated circuit has a connection for a clock signal CK. In line with the invention, a circuit arrangement 1 for measuring various operating parameters for the integrated circuit is connected to the external connections P0 to P2 and to the connection for the clock signal CK on the integrated circuit. The circuit arrangement 1 contains an analysis circuit 2 for detecting voltage level changes and an output circuit 3, in this case in the form of a controller. In this context, the analysis circuit 2 and the controller 3 are connected to one another for the purpose of interchanging data and control signals.

The analysis circuit 2 contains respective counter circuits 41, 51, 61, 71 which are connected directly or indirectly to one or more of the external connections P0 to P2. In addition, the analysis circuit 2 has a time counter circuit 91 which is connected to the connection for the clock signal CK and is used for logging a period of time. The time counter circuit 91 is in the form of a binary counter in the present embodiment, as are the rest of the counter circuits 41, 51, 61, and 71. Such a binary counter generally comprises a line of series-connected multivibrators in the form of flipflop circuits operating in succession. In this context, the states stored in the respective flipflop circuits represent a respective bit with a different significance in a digital value coded in this manner. In particular, the flipflop which receives the voltage level change on the respective connection represents the least significant bit, and the last flipflop in the flipflop line represents the most significant bit.

In the present exemplary embodiment, the counter circuits 41 and 51 are connected to the external connections P0 to P2 via a combinational logic circuit 8. In particular, the counter circuit 41 is connected to the external connections P0 and P1 via an OR gate 81, and the counter circuit 51 is connected to the external connections P1 and P2 via an AND gate 82. The counter circuits 61 and 71 are connected directly to the external connections P0 and P1, respectively, and thus count each voltage level change between the voltages V1 and V2 on the external connections P0 and P1. The time counter circuit 91 counts with each rising clock edge and in this way logs a period of time which can be used for averaging the digital values logged in the rest of the counter circuits.

Each of the counter circuits 41 to 91 has an associated register 42, 52, 62, 72 or 92 to which the respective digitally coded value 4, 5, 6, 7 or the time value 9 from the respective associated counter circuit is copied. The output signals a4, a5, a6, a7 and a9 are used to output the contents of these registers to the controller 3.

The combinational logic circuits 81, 82 are hardwired (integrated) or variably programmable. The latter means, by way of example, that the combinational logic circuits are produced semiflexibly by programmable simple AND, OR or exclusive-OR gates. In addition, the combinational logic circuits can be integrated in universally programmable form in a manner typical of GAL (Gate Array Logic). In this case, the procedure would be initiated by means of a test mode, in which case either the combinational logic circuit to be programmed or the counter register to be used would be addressed and a programming log would be used to store the evaluation logic which is to be programmed in a volatile or nonvolatile memory which controls the flexible combinational logic.

The mode of operation of the present embodiment of a circuit arrangement for measuring operating parameters is explained in more detail below.

At the start of measurement, the binary counters 41 to 91, which are 32 bits in length, for example, are reset to 0. The measurement can be started by a test mode, or the start is initiated by appropriately polling a start input pin provided for the purpose. In the present exemplary embodiment, the start of the measurement is initiated using the signal St on the controller 3. The measurement is stopped using a stop signal Sp on the controller 3, and the reset signal Rst is used to reset the respective counters. Following the start of measurement, each voltage level change between the voltages V1 and V2 on the external connections P0 and P1 is counted, or voltage level changes on a respective group combination of the external connections P0 to P2 are counted. The stop signal Sp immediately stops the counting process and then divides the values 4 to 7 from the corresponding counter circuits 41 to 71 by the time value 9 from the counter circuit 91. This division operation is brought about by a "shift right" operation on the respective contents of the counter circuits, which is equivalent to dividing by a multiple of the number 2. In this case, the shift right operation is determined by the content of the counter circuit 91 which logs the elapsed averaging time period. In this way, a set of characteristic averaged parameters up to a maximum error of the factor 2 is ascertained, with the parameters being able to be specified by virtue of multiple averaging.

An embodiment with more precise averaging which is improved in this regard provides for the current counter content to be copied to an associated register upon reaching an averaging

time which is a binary multiple. Such registers are shown in the Fig. using the registers 42, 52, 62, 72 and 92. These values stored in the registers are used to allow exact division by the averaging time which is a binary multiple. Another advantage is that the values stored in the registers 42 to 92 can be used for logged output at all times.

The log PK which is output by the controller 3 can include any binary-coded parameters, such as operating temperature, current drawn, voltage supply etc. In this context, transmission can take place in parallel, serially or in a combination of the two.

In one instance of application, the inventive circuit arrangement shown in the Fig. can be used, by way of example, to ascertain a set of operating parameters for an integrated memory circuit. In this case, the following are of interest, for example:

- how many voltage level changes take place per unit time on address, command and data pins,
- how many instruction changes take place per unit time,
- how many activation commands, preloading commands, write, read and refresh access operations are carried out,
- how many memory bank changes take place per unit time,
- how much noise the chip experiences when it is not being addressed,
- whether there is a certain rhythm in the addressing of the memory (for example "X-fast" or "Y-fast"),
- whether there is a certain rhythm in the instruction sequence,
- in what percentage the semiconductor memory is used for read and write access,
- how much operating current the memory chip draws.

These operating states can be calculated directly in the controller 3 using the individual logged parameters for the analysis circuit 2, or else the individual parameters are transmitted to the outside and are evaluated there.

Patent claims

1. A circuit arrangement for measuring at least one operating parameter for an integrated circuit,
- having an analysis circuit (2) which is connected to at least one external connection (P0 to P2) on the integrated circuit, with the analysis circuit detecting a plurality of voltage level changes (V1, V2) on the external connection and supplying them to a counter circuit (41 to 47) which logs at least one digitally coded value (4 to 7) which characterizes at least one operating parameter for specifying a mode of operation for the integrated circuit,
- having an output circuit (3), which is connected to the analysis circuit (2), for externally outputting the coded value or a value derived therefrom.

2. The circuit arrangement as claimed in claim 1, characterized in that
the external connection is used to control a method of operation for the integrated circuit.

3. The circuit arrangement as claimed in claim 1 or 2, characterized in that
the counter circuit (41 to 71) logs the voltage level changes over a defined period of time.

4. The circuit arrangement as claimed in one of claims 1 to 3,
characterized in that
- the analysis circuit (2) is connected to a plurality of external connections (P0 to P2) on the integrated circuit,
- the counter circuit (41, 51) is connected to the external connections via a combinational logic circuit (8).

5. The circuit arrangement as claimed in one of claims 1 to 4,
characterized in that
- the analysis circuit (2) is connected to a plurality of external connections (P0 to P2) on the integrated circuit and has a plurality of counter circuits (41, 51),
- each of the counter circuits is connected to one or more of the external connections via a different combinational logic circuit (81, 82) and respectively logs at least one digitally coded value.

6. The circuit arrangement as claimed in claim 4 or 5,
characterized in that
the combinational logic circuit (81, 82) is hardwired or is variably programmable.

7. The circuit arrangement as claimed in one of claims 1 to 6,
characterized in that
the or each of the counter circuits (41 to 71) has an associated register (42 to 72) to which a content of the respective associated counter circuit can be copied and stored.

8. The circuit arrangement as claimed in one of claims 1 to 7,
characterized in that
the analysis circuit (2) has a time counter circuit (91) which is connected to a connection for a clock signal (CK) for the purpose of logging a defined period of time.

9. A method for measuring at least one operating parameter for an integrated circuit,

- in which an analysis circuit (2) which is connected to at least one external connection (P0 to P2) on the integrated circuit is used to detect a plurality of voltage level changes (V1, V2) on the external connection and to log them in a counter circuit (41 to 71) using at least one digitally coded value (4 to 7),
- in which the coded value or a value derived therefrom is then output for analysis purposes in order to ascertain at least one operating parameter for specifying a mode of operation for the integrated circuit.

10. The method as claimed in claim 9,
characterized in that
- the analysis circuit (2) is connected to a plurality of external connections (P0 to P2) on the integrated circuit,
- the analysis circuit (2) is used to detect voltage level changes on the external connections (P0 to P2) in a plurality of different ways and to log them in a plurality of counter circuits using respective digitally coded values (4 to 7),
- a plurality of different operating parameters are ascertained from the digitally coded values.

11. The method as claimed in claim 9 or 10,
characterized in that
the digitally coded value(s) (4 to 7) are averaged.

12. The method as claimed in one of claims 9 to 11,
characterized in that,
upon reaching an averaging time which is a binary multiple during the measurement, the respective coded value (4 to 7) logged up till then is related to this averaging time.

Abstract

Circuit arrangement and method for measuring at least one operating parameter for an integrated circuit

A circuit arrangement for measuring at least one operating parameter for an integrated circuit contains an analysis circuit (2) which is connected to at least one external connection (P0 to P2) on the integrated circuit. The analysis circuit detects a plurality of voltage level changes (V1, V2) on the external connection, which is used to control a method of operation for the integrated circuit, in particular, and supplies them to a counter circuit (41 to 71) which logs at least one digitally coded value (4 to 7). The coded value is then output for analysis purposes in order to ascertain at least one operating parameter. This advantageously allows an average mode of operation for the integrated circuit to be logged during operation of the circuit in the application using parameters and allows respective operating states to be ascertained therefrom.

Fig.

nt

List of reference symbols

1	Circuit arrangement
2	Analysis circuit
3	Controller
4 to 7	Coded value
8	Combinational logic circuit
9	Time value
41, 51, 61, 71, 91	Counter
42, 52, 62, 72, 92	Register
81, 82	Gate
A4 to A9	Output signal
St	Start signal
Sp	Stop signal
Rst	Reset signal
PK	Log
P0 to P2	External connection
CK	Clock signal
V1, V2	Voltage